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**Reg. No. : .....**

**Name : .....**

# Sixth Semester B.Tech. Degree Examination, March 2015
## (2008 Scheme)
## 08.602 : VLSI Design (TA)
## (Special Supplementary)

Time : 3 Hours Max. Marks : 100



PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. Why is the oxidation rate of $\langle 111 \rangle$ wafer greater than $\langle 100 \rangle$ wafer ?
2. What are the different stopping mechanism in ion implantation ? What are the dominant stopping mechanism for Boron and Arsenic ?
3. What are the important criterion for hetero epitaxy of material A to be possible on a single crystal substrate of material B ?
4. What is boundary layer problem ? How can it be minimised in a horizontal epitaxy system ?
5. Implement an XOR gate using transmission gates.
6. Explain how the problem of charge leakage in dynamic logic rectified.
7. Explain velocity saturation. What is the effect of velocity saturation in short channel MOSFET ?
8. Discuss the constraints on the clock period and hold time for sequential circuits.
9. What are the functions of sense amplifier ?
10. Compare static and dynamic memory.

**(10×4=40 Marks)**

P.T.O.

## PART – B

Answer **two** questions from **each** Module.

### Module – I

11. a) Explain the different steps involved in photolithographic process for fabrications of IC, with necessary diagrams. 7

    b) Differentiate between positive and negative photo reset. 3

12. Illustrate the fabrication sequence of a CMOS inverter using SOI technology. What are the advantages it offers over conventional CMOS technology ? 10

13. Explain Czochralski technique for single crystal silcon growth. What are the disadvantages of the process which leads to the usage of float zone process for crystal growth ? 10

### Module – II

14. a) Implement the function F = AB (C + D) + DE using static CMOS technology. 5

    b) Why is domino logic preferred over simple dynamic logic ? Explain. 5

15. Explain accumulation, inversion and depletion in n channel MOSFET. What is the expression for threshold voltage ? What are the factors influencing the value of $V_T$ ? 10

16. a) Draw the DC characteristics of a CMOS inverter and explain. 7

    b) Find the expression for switching threshold. 3

### Module – III

17. Explain the working of SRAM cell and discuss how read and write operations are performed. 10

18. Implement a linear 16 bit carry select adder using 4 bit carry select adder blocks. How does a square root carry select adder improve the performance ? 10

19. Discuss the principle of Wallace Tree multiplier. How is the propagation delay reduced as compared to a simple array multiplier ? 10